REMARKS

Claims 1-12 stand rejected under § 102(b) as being anticipated by Shimomaki (U.S. Pub. No. 2002/0057243). Applicant traverses the rejection for the reasons below.

Regarding claim 1, applicant traverses the rejection because Shimomaki does not disclose that a gate signal is raised in a main scanning at a timing on or after a first inversion of a data signal occurring during a selected horizontal scanning period, and the gate signal is broken down in the main scanning at a timing prior to the next following inversion of the data signal occurring during the selected horizontal scanning period.

The examiner appears to assert that the "n-th FIELD" shown in Figs. 2A-2C of Shimomaki corresponds to the selected horizontal scanning period recited in the claims. However, the field period is different from a horizontal scanning period. An active matrix type liquid crystal display generally includes a plurality of gate lines which are scanned sequentially. In Shimomaki, the time required to scan all gate lines sequentially is referred to as one frame period, and each frame period is divided into two field periods. Thus, in Shimomaki, one field period represents the period of time in which half of the plurality of gate lines is scanned. For example, Figs. 2A-2C of Shimomaki show that three lines are scanned during the n-th FIELD period.

In contrast, the present specification defines one horizontal scanning period as the period in which one gate line is scanned. Thus, one field period of Shimomaki includes a plurality of horizontal scanning periods as defined by the present specification. Therefore, Shimomaki fails to disclose or suggest the claimed features of the gate signal as described in

claim 1. For this reason, applicant requests withdrawal of the rejection of claim 1, and its associated dependent claims.

Regarding claim 3, applicant traverses this rejection because Shimomaki fails to disclose that an on-voltage of a gate signal in the pre-scanning has a value that is different that that of an on-voltage of the gate signal in the main scanning.

The examiner asserts that Shimomaki discloses value $\Delta v1$ and $\Delta v2$ which are different. However, as shown in Fig. 2A, $\Delta V1$ represents the difference between the black signal voltage Vmax and the liquid crystal application voltage Vp1, while $\Delta V2$ indicates the difference between the display signal voltage Vsig and the liquid crystal application voltage Vp1. Applicant submits that neither of these values represents an on-voltage of a gate signal. However, Fig. 2A does show a scanning signal voltage Vg which corresponds to a gate signal voltage. As shown in Fig. 2A, during time periods Ta and Tb, which the examiner asserts correspond to pre-scanning and main scanning, respectively, the value of scanning signal Vg corresponds to an amount labeled ΔVg. That is, the value of the scanning signal in the pre-scanning is the same as the value of the scanning signal in the main scanning.

In contrast, as shown in Fig. 21 of the present specification, the gate signal has a value Vgon1 during pre-scanning period B and a value Vgon2 in the main scanning period A. Thus, in the present invention, the value of a gate-on voltage of the gate signal in the pre-scanning period is different than the gate value of the gate-on voltage of the gate signal in the main scanning period. For this reason, applicants respectfully request withdrawal of the rejection of claim 3.

Regarding claim 4, applicant traverses this rejection because Shimomaki fails to disclose that a length between the raising of a gate signal and the timing of a next following breaking down of the gate signal in the pre-scanning period is different from that in the main scanning period.

As shown in Fig. 21 of the present application, the main scanning period A is shorter than the pre-scanning period B. That is, the timing between the rising of the gate signal 28 at the beginning of pre-scanning period B and the breaking down of the gate signal at the end of pre-scanning period B is different than the amount of time between the raising of the gate signal and the next breaking down of the gate signal at the beginning and the end of main scanning period A.

In contrast, Shimomaki is silent regarding the lengths of periods Ta and Tb as shown in Fig. 2A. However, in paragraph [0067] lines 4-5, Shimomaki teaches that the widths of gate pulses P1 and P2 (which correspond to periods Ta and Tb, respectively) are each 30 microseconds. That is, Shimomaki discloses that the length of time between the raising of the gate signal Vg and the next following breaking down of the gate signal during the gate pulse P1 is the same as that during the gate pulse P2, and not that the length of time is different as required in claim 4. For this reason, applicant respectfully requests withdrawal of the rejection of claim 4.

Regarding claim 5, applicant traverses the rejection because Shimomaki does not disclose using a data signal whose polarity is inverted for every horizontal scanning period.

As discussed with regard to claim 1, a horizontal scanning period is the period of time in which one gate line is scanned. As shown, in Fig. 9 of the present specification, each inversion of data signal 26 (i.e., each time the data signal crosses the center of the data signal 27) marks the beginning of a new horizontal scanning period. Thus, it is clear that the polarity of the data signal is inverted for each horizontal scanning period in the present invention.

As shown in Fig. 2A of Shimomaki, the display signal Vsig is inverted at the beginning of each field period. However, as discussed above, each field period includes multiple horizontal scanning periods. Thus, Shimomaki fails to disclose that a data signal's polarity is inverted for each horizontal scanning period. For these reasons, applicant respectfully requests withdrawal of the rejection of independent claim 5 and its respective dependent claims.

Regarding claim 11, applicant traverses the rejection because Shimomaki fails to disclose that a value of a gate-off voltage between a pre-scanning period and the main scanning period is set to be higher than a value of the gate-off voltage after the main scanning period.

The examiner asserts that voltage Vp1 of Shimomaki corresponds to a gate-off voltage of the present invention. However, Vp1 represents the voltage applied to the liquid crystal, while voltage Vg represents the scanning signal. Accordingly, applicant asserts that the scanning signal Vg more closely corresponds to the gate voltage of the present invention. As shown in Figs. 2A-2C of Shimomaki, the value of the scanning signal Vg during the

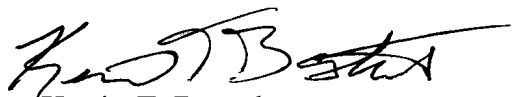
period Tp (i.e., the time between periods P1 and P2) is equivalent to the value of scanning signal Vg after the period P2.

In contrast, as shown in Fig. 8 of the present specification, the value of gate signal 28 between the pre-scanning period B and main scanning period A is 0 volts. After the main scanning period A, gate signal 28 reaches an even lower gate-off voltage having a value of -5 volts. Thus, the gate-off voltage between the pre-scanning period B and the main scanning period A is higher than the gate-off voltage after the main scanning period. Because Shimomaki fails to disclose this feature, applicant respectfully requests withdrawal of the rejection of claim 11 and its respective dependent claims.

For all the foregoing reasons, applicant submits that this application is in condition for allowance, which is respectfully requested. The examiner is invited to contact the undersigned attorney if an interview would expedite prosecution.

Respectfully submitted,

GREER, BURNS & CRAIN, LTD.

By 

Kevin T. Bastuba
Registration No. 59,905

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300 South Wacker Drive
Suite 2500
Chicago, Illinois 60606
Telephone: 312.360.0080
Facsimile: 312.360.9315

Customer No. 24978